JHARKHAND Rai University
UGC RECOGNISED UNIVERSITY
ACCREDITED BY NAAC

Lesson Plan & Tracking

Programe : MCA	**Session : 2022 - 2024**	**Year : 2022**	**Sem: 1st**
Course: Computer Organization & Architecture			
Name of the Faculty: Rajan Kumar Tiwari	**Commencement Date: 29.08.2022**		**Date of Closure: 30.12.2022**

Lecture No.	Week	Unit	Topics to be Covered	Blended Mode			Date	Duration	Tracking of Lectures	Related Course Outcome	Signature of Faculty	Signature of HoD	Remarks (if any)
				ICT Tool/Platform/ LMS	Resources	Activity							
1	1	1	Discussion on syllabi and course objective-outcome										
2		1	Axioms and laws of Boolean algebra, Reduction of Boolean expressions										
3		1	Conversion between canonical forms, Karnaugh map										
4	2	1	K- map (4 variable),										
5		1	Half Adder, full adder										
6		1	4-bit parallel parity bit generator, checker circuit										
7	3	1	Decoder, Encoder, Multiplexer										
8		1	IC RAM, ROM										
9		1	Memory Organization, Sequential Circuits, State transistors,										
10	4	1	Flip-flop, RS, JK, D-Latch, Masterslave										
11		1	Byte Addressability, Big-Endian										
12		2	Little-Endian Assignments										
13		2	Word Alignment, Instructions and Instruction Sequencing,										
14		2	Addressing Modes,Assembly Language,										

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15	5	2	Addressing Modes										
16		2	Subroutines, Additional Instructions, dealing with 32-Bit Immediate Values										
17	6	3	Some Fundamental Concepts,										
18		3	Instruction Execution, Hardware Components										
19		3	Instruction Fetch and Execution Steps										
20	7	3	Control Signals, Hardwired Control,										
21		3	CISC Style Processors										
22		3	Pipelining: Basic Concept, Pipeline Organization										
23	8	3	Pipelining Issues, Data Dependencies,										
24		4	Memory Delays, Branch Delays										
25		4	Pipeline Performance Evaluation.										
26	9	4	Basic Concepts, Semiconductor RAM Memories, Read-only Memories										
27		5	Direct Memory Access,										
28		5	Memory Hierarchy, Cache Memories, Virtual Memory										
29	10	5	Memory Management Requirements, Secondary Storage										
30	10	5	input output basic,bus structure,operation										
31	10	5	arbitration, interconnection standard										
32	10	5	parallel processing ,SIMD,Mutiprocessor, performance Modelling										

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				ICT Tool/Platform/ LMS	Resources	Activity							
33	10	5	parallel processing ,SIMD, Mutiprocessor										
34	10	5	Performance Modelling										
35	10	5	Model paper discussion										
36	10	5	Model paper discussion										